SAMPA Specification
MPW1

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Revision

0.1 Initial draft

0.2 Added reset tree and description of reset procedure

0.3 Minor fix in table 2.3

Contents

Chapter 1

Interfaces

This section describes the protocols and properties of the various interfaces for the SAMPA MPW1.

1.1 Slow Control

The slow control of the MPW1 SAMPA ASIC is done through a simple full-duplex serial interface. The interfaces uses one RX and one TX line at LVCMOS 1.5 V clocked in relation to the ADC clock. Pin positioning is given in table 1.1. As the protocol includes device addressing the interface can be used in a multi-drop bus fashion.

Pin	Name in code	Mode	Block
120	instr_serial_out	O	DSP
121	instr_serial_in	I	DSP

Table 1.1: *Pin list relevant for MPW1 slow control interface*

The input and output lines are normally low and a message is initiated by one start bit. The data is sent LSB first and is read by the SAMPA on the rising edge of the clock. The protocol is shown in table 1.1 with the description in table 1.2.
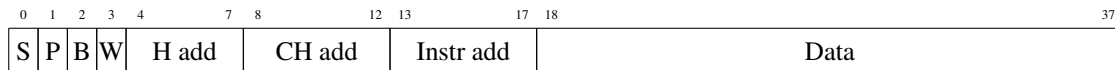
Figure 1.1: *Format of data sent to the SAMPA.*

Name	Bits	Description
S	1	Start bit, always 1
P	1	Parity (odd) of packet excluding the start bit
B	1	Broadcast bit, instruction written to all channel addresses if 1
W	1	1=Write to address, 0=Read
H add	4	Hardware address of chip
CH add	5	Channel address, irrelevant when broadcast=1
Instr add	5	Register address
Data	20	Register data to be written

Table 1.2: *Protocol bit field descriptions of data sent to the SAMPA.*

After a message has been received by the SAMPA, it will answer after 4 clock cycles unless one of the following error conditions has occurred:

- Parity error.

- Wrong hardware address.

- Reading of data from a channel specific register and broadcast is enabled.

- Writing of data to a read only register.

- Requested register does not exist.

Data is sent with one start bit and the data as LSB first. The data is written from the SAMPA on rising edge of the clock.
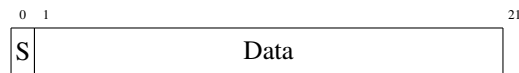

Figure 1.2: *Format of data sent from the SAMPA.*

Name	Bits	Description
S	1	Start bit, always 1
Data	20	If command message = 0x55555 (ACK)
		If write message = data at written register after write[1]
		If read message = data at requested register

Table 1.3: *Protocol bit field descriptions of data sent from the SAMPA.*

1.2 Serial interface

The SAMPA MPW1 is equipped with four LVCMOS 1.5 V serial links clocked in relation to the serial clock provided by the interfacing device. The IO pads available for MPW1 are limited to 129 MHz at 20 pF load (348 MHz at 0.05 pF) resulting in a probable maximum of 260 MHz for the input serial clock, though experimental testing needs to confirm this. The SAMPA can still be supplied with the designed 320 MHz serial clock as long as the integrity of the output serial data is of no concern, for instance for noise testing purposes of the analog part. The relevant pins for the serial interface is shown in table 1.4.

1.2.1 Configurtation

The number of active serial links can be set by the hardware pins MPW1_numserialOut[1:0], see table 1.5 for configuration. The setting is also available through the registry, but it has no effect for the MPW1 as the hardware pins take precedence.

1.2.2 Protocol

The data sent from the SAMPA consists of a fixed length header and a variable length data payload. The combined header and payload is here on referred to as a packet. The data is written LSB first on rising edge of the clock. The data payload contains zero suppressed and run length encoded samples in a back linked list in the same way as for the previous ALTRO chip.

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[1]Since not all bits in a register is always writable, the data returned might not be the same as written

Pin	Name in code	Mode	Description
145	SerialOut0	O	Serial link
144	SerialOut1	O	Serial link
143	SerialOut2	O	Serial link
142	SerialOut3	O	Serial link
126	MPW1_numserialOut[0]	I	Serial link disabler
127	MPW1_numserialOut[1]	I	Serial link disabler
138	hb_trg	I	Heartbeat trigger
139	trg	I	Event trigger
140	sync	I	Bunchcrossing sync

Table 1.4: *Pin list relevant for MPW1 serial interface*

1 : 0	Configuration	Active serial links	Channel => links
00	1 link	0	0–31 => 0
01	2 links	0, 2	0–15 => 0, 16–31 => 2
10	4 links	0, 1, 2, 3	0–7 => 0, 8–15 => 1, 16–23 => 2, 24–31 => 3
11	0 links	N/A	N/A

Table 1.5: *MPW1_numserialOut[1:0] configuration*

0	7 8 9 10 11	14 15	19 20	29 30	49
Preamble	P E T	H add	CH add	Num words	BX count

Figure 1.3: *Format of serial data header.*

Name	Bits	Description
Preamble	8	0x33 (0b00110011)
P	1	Parity (odd) of header
E	1	Early trigger, trigger received before end of timewindow
T	1	Data truncated due to overflow (0 data following)
H add	4	Hardware address of chip
CH add	5	Channel address
Num words	10	Number of 10 bit words in data payload
BX count	20	Bunch-crossing counter (40MHz counter)

Table 1.6: *Protocol bit field descriptions of data sent from the SAMPA.*

0 50	
Header	Payload

Figure 1.4: *Format of serial data. Length of payload is variable and given in the header information.*

1.2.3 Heartbeat packet

Heartbeat packets are specially crafted packets that have the same length as a header (50 bits), but only contains the bunchcrossing counter and the header in addition to the parity and preamble. They are initiated by a single pulse on the heartbeat trigger pin (hb_trg) and the bunchcrossing counter is saved the moment the trigger is detected.

The heartbeat packets are only sent on serial link 0 and has the highest priority, it will be sent after the

transmission of the current packet has been completed. The heartbeats have no practical purpose for the MPW1.

0	24 25 26	29 30	49
Preamble	P	H add	BX count

Figure 1.5: *Format of heartbeat packet.*

Name	Bits	Description
Preamble	25	0xF83E0F (0b1111100000011111000001111)
P	1	Parity (odd) of header
H add	4	Hardware address of chip
BX count	20	Bunch-crossing counter (40MHz counter)

Table 1.7: *Protocol bit field descriptions of heartbeat packet.*

Heartbeat trigger

This is the trigger signal for the heartbeat packet. It is sampled on the rising edge of the 40 MHz bunch crossing clock.

1.3 Test interfaces

Various test interfaces are available to ease both functional and radiation testing of the SAMPA.

1.3.1 Shift register

The shift register is intended to investigate the cross-section and sensitivity of the The shift register contains 15k (15000 ?!?) shift registers of the smallest and weakest flip-flops available connected in series with separate ground and powersupply. VDD33 supplies voltage to the IO pads while VDD supplies voltage to the flip-flops. The flip-flops capture on the are falling edge of the clock.

The clocking speed is limited by the drive capacity of the IO pads to the same as serial output link of 129 MHz, though experimental testing is needed to confirm this.

Pin	Name	Mode	Function
186	si	I	Data in first flip-flop
187	so	O	Data out last flip-flop
188	clk	I	Clock
185	VSS	GD	Ground
190	VSS	GD	Ground
184	VDD33	PR	3.3V I/O
189	VDD	PC	1.2V Core

Table 1.8: *Pin list relevant for MPW1 shift register*

1.3.2 DSP test interfaces

Extra test interfaces are available to investigate the filter functionality and the raw data from the ADC's as can be seen in figure 1.6.

Pin	Name	Mode	Function
82	MPW1_dinOUTSIDE[9]	I	Test data input
83	MPW1_dinOUTSIDE[8]	I	Test data input
84	MPW1_dinOUTSIDE[7]	I	Test data input
85	MPW1_dinOUTSIDE[6]	I	Test data input
86	MPW1_dinOUTSIDE[5]	I	Test data input
87	MPW1_dinOUTSIDE[4]	I	Test data input
91	MPW1_dinOUTSIDE[3]	I	Test data input
117	MPW1_dinOUTSIDE[2]	I	Test data input
118	MPW1_dinOUTSIDE[1]	I	Test data input
119	MPW1_dinOUTSIDE[0]	I	Test data input
122	MPW1_Selectin	I	Select test data or ADC 1
123	MPW1_enBC1	I	Enable CH 0 BC1
124	MPW1_enBC2	I	Enable CH 0 BC2
125	MPW1_enZSU	I	Enable CH 0 ZSU
130	MPW1_selectOut[2]	I	Select for test-output mux
131	MPW1_selectOut[1]	I	Select for test-output mux
132	MPW1_selectOut[0]	I	Select for test-output mux
169	MPW1_dout[12]	O	Test data output
170	MPW1_dout[11]	O	Test data output
171	MPW1_dout[10]	O	Test data output
172	MPW1_dout[9]	O	Test data output
173	MPW1_dout[8]	O	Test data output
174	MPW1_dout[7]	O	Test data output
175	MPW1_dout[6]	O	Test data output
176	MPW1_dout[5]	O	Test data output
177	MPW1_dout[4]	O	Test data output
178	MPW1_dout[3]	O	Test data output
179	MPW1_dout[2]	O	Test data output
180	MPW1_dout[1]	O	Test data output
181	MPW1_dout[0]	O	Test data output

Table 1.9: *Pin list relevant for MPW1 test interfaces*

DSP channel 0 input selection

A multiplexer has been set up to select between ADC 1 and an external supplied digital signal.
Setting MPW1_Selectin to 0 selects the data from ADC 1.
Setting MPW1_Selectin to 1 selects the data from MPW1_dinOUTSIDE.

DSP channel 0 filter bypass

The three filters BC1, BC2 and ZSU for DSP channel 0 can be disabled through external pins. TCFU is disabled by default.

MPW1_enBC1 Setting this to 0 overrides the BC1_CFG part of the Data Path Configuration DPCFG[3:0] register for channel 0 to b0000. This does not disable the BC1 filter, but sets the input polarity to positive and the operating mode to $din - fixed pedestal$. The fixed pedestal is default 0 on startup.

MPW1_enBC2 Setting this to 0 sets bit 11 of DPCFG to 0 for channel 0, which is the bit to enable the second baseline correction.

MPW1_enZSU Setting this to 0 sets the zero suppression threshold to 0 for channel 0.

Test-output multiplexer

Internal data from the channel 0 DSP or from the 3 ADC's can be brought out to external pins through a multiplexer. The multiplexer is controlled by MPW1_selectOut and the configuration can be seen in table 1.10.

MPW1_selectOut[2 : 0]	Output value
000	CH 0 BC1
001	CH 0 TCFU
010	CH 0 BC2 *
011	CH 0 ZSU *
100	ADC 1 *
101	ADC 2 *
110	ADC 3 *
111	0

Table 1.10: *MPW1_dout[12:0] configuration. Those marked with * has been the zero padded to 13 bits for the MSBs.*
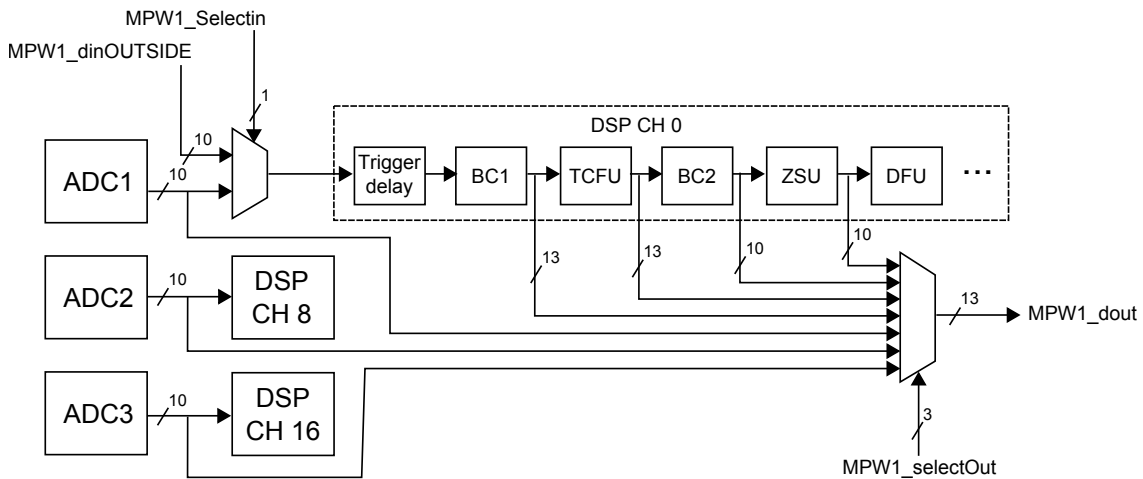
Figure 1.6: *Block diagram of MPW1 DSP test interfaces.*

1.4 Misc interfaces

1.4.1 Hardware address

The hardware/chip address for the device can be set with hadd[3:0] between 0 and 15. This is use by both the slow control and serial interface.

Pin	Name	Mode	Description
78	hadd[3]	I	Chip address
79	hadd[2]	I	Chip address
80	hadd[1]	I	Chip address
81	hadd[0]	I	Chip address

Table 1.11: *Hardware address*

1.4.2 BX synchronization, event- and heartbeat trigger

Three inputs are provided for sync and triggering. They are all sampled on the rising edge of the 40 MHz bunch crossing clock.

hb_trg Upon a pulse, the current BX counter value is captured and a heartbeat packet is crafted.

trg This is the event trigger for use when running in triggered mode.

sync This only resets the bunch crossing counter.

Pin	Name	Mode	Description
138	hb_trg	I	Heartbeat trigger
139	trg	I	Event trigger
140	sync	I	Bunchcrossing sync

Table 1.12: *BX sync, event- and heartbeat trigger pins*

1.4.3 Clock and reset

The pins clock and reset pins are given in table 1.13.

Pin	Name	Mode	Description
128	clk10in	I	ADC clock (10-20 MHz)
129	clk40in	I	Bunch crossing clock (40 MHz)
141	clk320in	I	Serial link clock (up to 320 MHz)
137	Hrstb	I	Hard reset

Table 1.13: *Clock and reset pins*

Clock

There are four clock domains in the SAMPA;

- The ADC clock controls the acquisition of data from the ADC and acts as the main clock for the DSP channels from the input to the ringbuffer.

- Between the ringbuffer and the serial out is the serial link word-clock, which is the serial link clock divided by 10.

- The 10 bit words are shifted out the serial link with the serial link clock.

- A bunch crossing counter is implemented which operates on the LHC bunch crossing clock.

Reset

The reset tree is implemented as shown in figure 1.7. The reset is active low and the pulse needs to be longer than one serial link clock cycle. The reset takes (2x serial link clock cycle + 2x BX clock cycle + 2x serial link /10 clock cycle + 2x ADC clock cycle) in a worst case condition depending on the phase of the different clocks. For the standard clockrates of 320 MHz, 40 MHz, 32 MHz, 10 MHz this amounts to a maximum of 320 ns. For more optimal phase differences the reset time would be halved.

A software reset is available through the instruction interface as shown in figure 1.8. The signal is synchronized to each clock domain before being combined with the hardware reset signal.
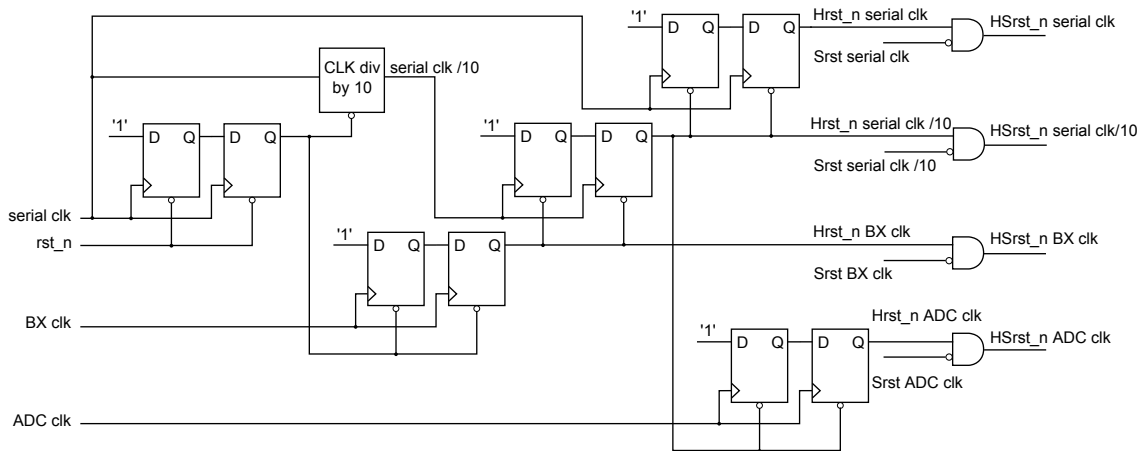
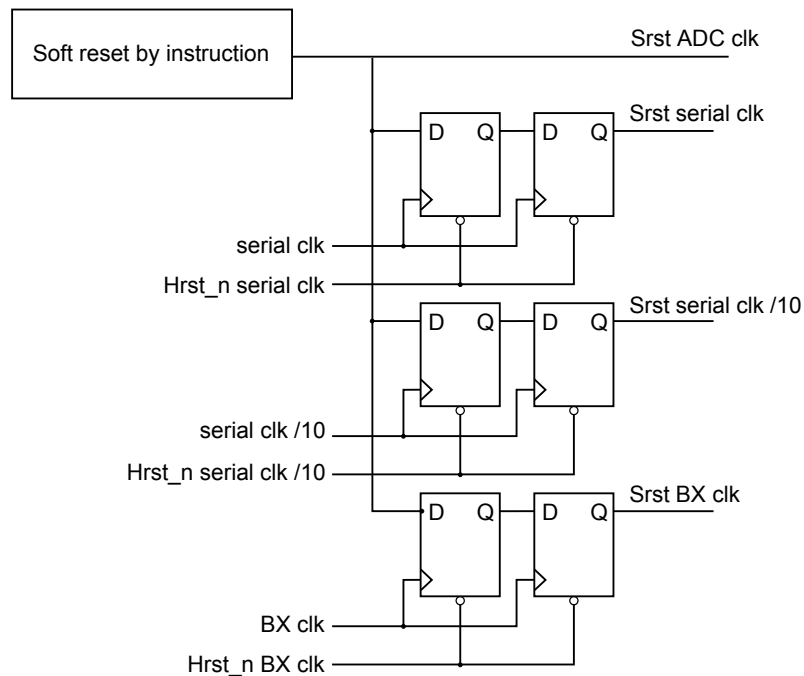**Figure 1.7:** *Block diagram of MPW1 hardware reset tree.*

Figure 1.8: *Block diagram of MPW1 software reset tree.*

Chapter 2

Registers

2.1   Channel specific registers

These are registers specific to each channel. By using a broadcast command, all channels can be written at the same time.

Register name		Address	Type	Default value		Description
K1	[12:0]	0x00	RW	0x00	[12:0]	First pole of the TCFU
K2	[12:0]	0x01	RW	0x00	[12:0]	Second pole of the TCFU
K3	[12:0]	0x02	RW	0x00	[12:0]	Third pole of the TCFU
K4	[12:0]	0x03	RW	0x00	[12:0]	Fourth pole of the TCFU
L1	[12:0]	0x04	RW	0x00	[12:0]	First zero of the TCFU
L2	[12:0]	0x05	RW	0x00	[12:0]	Second zero of the TCFU
L3	[12:0]	0x06	RW	0x00	[12:0]	Third zero of the TCFU
L4	[12:0]	0x07	RW	0x00	[12:0]	Fourth zero of the TCFU
ZSTHR	[19:0]	0x08	RW	0x0A	[9:0]	Zero suppression threshold
			RW	0x00	[19:10]	Zero suppression offset
ZSCFG	[6:0]	0x09	RW	0x02	[1:0]	Glitch filter, minimum accepted pulse
			RW	0x07	[4:2]	Post-samples
			RW	0x03	[6:5]	Pre-samples
VFPED	[19:0]	0x0A	RW	0x00	[9:0]	BC1 Fixed pedestal
			R	0x00	[19:10]	BC1 variable pedestal
CTE	[9:0]	0x0B	RW	0x00	[9:0]	Channel specific noise
PMDTA	[9:0]	0x0C	RW	0x00	[9:0]	Data to be stored in the pedestal memory

Table 2.1: *Channel specific registers*

2.2   Global registers

These are global registers and does not accept broadcast commands.

Register name		Address	Type	Default value		Description
PMADD	[9:0]	0x0D	RW	0x00	[9:0]	Pedestal memory address
BC2THR	[19:0]	0x0E	RW	0x03	[8:0]	Lower threshold of moving average filter
			RW	0x03	[17:9]	Higher threshold of moving average filter
			RW	0x01	[19:18]	Number of taps in moving average filter
TRCFG	[19:0]	0x0F	RW	0x00	[7:0]	Number of pre-samples (Pretrigger delay), max 191
			RW	0x3FD	[17:8]	Number of samples per event, max 1021
DPCFG	[11:0]	0x10	RW	0x00	[3:0]	BC1 mode, see ALTRO manual
			RW	0x00	[4]	BC1 polarity
			RW	0x07	[6:5]	BC2 pre-samples
			RW	0x07	[10:7]	BC2 post-samples
			RW	0x01	[1]	BC2 moving average filter enable
VACFG	[7:0]	0x11	RW	0x00	[1:0]	Number of neighbors, not in use
			RW	0x01	[3:2]	Number of serial out, see table 1.5
			RW	0x00	[4]	Pedestal mode enabled (zero suppression threshold 0)
			RW	0x01	[5]	Power save mode enabled
			RW	0x00	[6]	TCFU enabled
			RW	0x01	[7]	Continuous mode enabled
BC1THR	[13:0]	0x12	RW	0x03	[4:0]	Lower threshold of variable pedestal filter
			RW	0x03	[9:5]	Higher threshold of variable pedestal filter
			RW	0x01	[13:10]	Number of taps in variable pedestal filter
TRCNT	[15:0]	0x13	R	0x00	[15:0]	Trigger count
HWADD	[4:0]	0x14	R	0x00	[4:0]	Chip address (hardware address)
ERRORS	[5:0]	0x15	R	0x00	[0]	Parity error in received instruction
			R	0x00	[1]	Instruction error
			R	0x00	[2]	Trigger overlap
			R	0x00	[3]	SEU in MMU SM (not implemented)
			R	0x00	[4]	SEU in interface SM (not implemented)
BXCNT	[19:0]	0x16	R	0x00	[19:0]	Bunch crossing counter

Table 2.2: *Global registers*

2.3 Command registers

These are command registers and can only be written to. The value doesn't matter as only the access is detected.

Register name	Address	Type	Description
SWTRG	0x1B	W	Software trigger (not implemented)
TRCLR	0x1C	W	Clear trigger counter
ERCLR	0x1D	W	Clear errors
BXCLR	0x1E	W	Clear bunch crossing counter
SRST	0x1F	W	Software reset

Table 2.3: *Command registers*